Amendments to the Specification

Page 2:

Please substitute the following paragraph for the paragraph beginning at line 5:

More specifically, as shown in Fig. 11, data such as 1 word (16 bits), supplied from the microprocessor via buses BUS0 through BUS15 are successively taken into latch circuit groups LTG1 through LTG4, provided to match bit lines of the display RAM 140, in synchronism with timing signals ϕ11, ϕ12 ... shown in Fig. 12. Transfer gate groups TGT1 through TGT4, provided between the latch circuit groups LTG1 through LTG4 and the display RAM, are successively opened in accordance timing signals ϕ31, ϕ32 ..., and data are successively written into the display RAM 140 word by word. This has been the usual way [[or]] of processing.

Page 3:

Please substitute the following paragraph for the paragraph beginning at line 5:

However, among mobile electronic apparatuses, since mobile telephones in particular need battery saving, the display control device and other LSIs (large scale

integrated circuits) to be mounted on them are required to be reduced in power consumption. Yet, as the display RAM built into a conventional display control device uses a system in which data are sequentially written word by word as shown in Fig. 12, a problem has been found that, if the write speed is to be raised to match the transfer speed of display data from the microprocessor, the power consumption will increase in proportion to the transfer speed.

Please substitute the following paragraph for the paragraph beginning at line 23:

~~What follows is a brief summary of a typical aspect of~~ In accordance with one of its principal aspects, the present invention ~~disclosed in this application. Thus,~~ provides a display control device ~~provided with~~ having a display memory which is capable of storing display data for a display device and into which display data are written in a prescribed number of bits at a time~~, the~~. The display control device successively ~~reading~~ reads display data out of the display memory and ~~forming and supplying~~ forms and supplies a drive signal to the display device~~, wherein the~~. The display memory has a memory array provided with a plurality of memory cells arranged~~,~~

~~well ordered in vertical and horizontal directions,~~ in an array, a plurality of word lines to which selection terminals for the memory cells of the same row are connected, and a plurality of bit lines which are arranged in a direction to cross the word lines and to which data input/output nodes for memory cells of the same column are connected~~; input~~. Input transfer means and output transfer means are connected to the bit lines[[;]], and data ~~transferring~~ transfer by the input transfer means results in writing of data into memory cells connected to a word line in a selected state~~; and~~, whereas data ~~transferring~~ transfer by the output transfer means results in reading of data out of memory cells connected to a word line in a selected state[[,]]. The display control device is further provided with a plurality of first data latch means capable of successively taking in display data in the prescribed number of bits at a time~~, and display~~. Display data held by the first data latch means can be collectively transferred by the input transfer means to the bit lines of the display memory in a number of bits at a time equal to an integral multiple of (n times) the number of bits of the display data taken into the first data latch means.

Page 5:

Please substitute the following paragraph for the paragraph beginning at line 1:

[[The]] In the device described above, ~~in which~~ the display memory has a configuration without sense amplifier, ~~namely a configuration in which data~~. Data to be written into the display memory are transferred by the input transfer means from the latch circuit directly to a bit line and, when data are to be read, data on a bit line are supplied by the output transfer means and a plurality of data are collectively written into the display memory are being once latched by the latch circuit[[,]]. This can save ~~power consumption~~ as much power as a sense amplifier would otherwise consume~~, and the~~. The power consumption by the memory can also be reduced as compared with a system in which data are written one by one into the display memory, because the frequency of accessing the display memory (the frequency of actuating word lines) is reduced. ~~The dispensation~~Dispensing with a sense amplifier, even though it may slow down writing or reading, results in faster overall data writing than the conventional system of writing data one by one, because a plurality of data can be written into the display memory collectively.

Please substitute the following paragraph for the paragraph beginning at line 19:

Preferably, the display control device may be further provided with a plurality of second data latch means. The second data latch means are capable of taking in display data held by the first data latch means in a number of bits at a time equal to an integral multiple of the number of bits of the display data taken into the first data latch means~~, wherein~~. Further, the input transfer means are configured to be capable of transferring display data held by the second data latch means to the bit lines of the display memory in a number of bits at a time equal to an integral multiple of (n times) the number of bits of the display data taken into the first data latch means. As this enables[[,]] the display data to be written next to be taken in by the first data latch means while the data to be written into the display memory are transferred from the second data latch means to the display memory, ~~the display data to be written next to be taken in by the first data latch means,~~ data can be written at high speed even when writing of data into memory cells connected to the same bit line is to take place consecutively.

Page 6:

Please substitute the following paragraph for the paragraph beginning at line 11:

Also preferably, transferring of data by the input transfer means to the bit lines of the display memory may take place at the same timing as the final data are taken into the first data latch means. ~~This enables~~Thus, even when data to be written into the display memory are to be transferred in a number of bits at a time equal to an integral multiple of the prescribed number of bits, the data can be transferred one cycle earlier than where they are transferred to the display memory collectively in the next cycle after the final data are taken into the first data latch means.

Please substitute the following paragraph for the paragraph beginning at line 21:

Also, the number of the first data latch means is an integral multiple ~~further of the~~ n times. ~~This enables~~Thus, where data are to be written consecutively onto one row of the display memory, the data can be

transferred without generating any fraction and the total time length of data writing to be shortened.

Page 8:

Please substitute the following paragraph for the paragraph beginning at line 24:

In the mobile electronic apparatus, the display control device may be provided with a segment drive means for generating signals for driving segment electrodes of the liquid crystal display device, and a common electrode drive circuit for generating a signal for driving common electrodes of the liquid crystal display device is configured as a semiconductor integrated circuit over a separate semiconductor chip from the semiconductor chip over which the display control device is formed, wherein the common electrode drive circuit is configured of an element higher in withstand voltage than the elements constituting the display control device. This enables only the common electrode drive circuit requiring a high withstand voltage to be configured [[of]] on another chip, making it possible to enhance the performance compared with a configuration in which segment drive means and the common

electrode drive circuit are formed over the same chip, to simplify the process and to reduce the manufacturing cost.

Page 13:

Please substitute the following paragraph for the paragraph beginning at line 5:

Further in the system of this configuration, a segment driver for driving ~~(e.g. 384)~~ segment electrodes (for example, 384 segment electrodes) of the liquid crystal panel 10 is built into the liquid crystal control driver 100, and a common driver 70 for driving ~~(e.g. 176)~~ common electrodes (for example, 176 common electrodes) of the liquid crystal panel 10 is configured over another semiconductor chip. However, this configuration is not absolutely required, but the liquid crystal control driver 100 may have both a segment driver and a common driver built into it as illustrated in Fig. 1(B) for example.

Please substitute the following paragraph for the paragraph beginning at line 17:

This example of liquid crystal control driver 100 is provided with a pulse generator 110 for generating a reference clock pulse within the chip on the basis of an

oscillation signal from an external source or an oscillation signal from an oscillator connected to an external terminal, a timing generator 111 for generating a timing control signal within the chip on the basis of this clock pulse, a control unit 120 for controlling the whole chip inside in accordance with an instruction from the external microprocessor 53, a system interface 131 for transmitting and receiving data to and from the microprocessor 53, a common driver interface 132 for supplying the external common driver chip 70 with a control signal CS, a clock signal CCL, a command CDM and so forth, and a display random access memory (RAM) 140 as a display memory for storing display data in a bit map system. The display RAM is configured [[of]] with 176 word lines × 1024 bits for instance, and operates at a speed of about 2 MHz.

Page 19:

Please substitute the following paragraph for the paragraph beginning at line 19:

Fig. 4 illustrates a specific example of memory array 141 and transfer gate groups TGT. In the memory array 141, a plurality of word lines W0, W1 ... and complementary bit lines BL0, /BL0; BL1, /BL1 ... are arranged in mutually

crossing directions, and a memory cell MC is arranged in each of the boxes formed by the word lines W0, W1 ... and the complementary bit lines BL0, /BL0; BL1, /BL1 ... The memory cells MC are static memory cells of the known six-element type, and a pair of input/output terminals of each memory cell MC are connected to one of the complementary bit lines BL0, /BL0; BL1, /BL1 ...; BL15, /BL15, and the selection terminal of each memory cell MC is connected to one of the word lines W0, W1... .

Page 30:

In Fig. 9(B), blank boxes (□ marks) signify data to be written, and ~~blank~~ filled-in boxes (■ marks), data to be masked. In both cases, data to be written from the external microprocessor into the first latch groups LTG11 through LTG14 are data of 12 words. Fig. 9(C) shows values to be set into the mask register 122 to match cases 1 through 4. The end address may as well be the leading address "0008" of the final group instead of "000B".

IN THE ABSTRACT

Please replace the original Abstract with the accompanying Abstract on a separate sheet.